

PATENT**IBM Docket No. RAL919970043US5****Amendments to the Claims:**

1-29. (Canceled)

30. (Currently Amended) A LAN emulation system comprising:a plurality of local area networks (LANs);an ATM network;a plurality of LAN switches for interconnecting LANs and ATM networks;a controlling processor; anda LAN emulation means, wherein communications in the form of frames are transmitted from a first LAN to the LAN switch to the ATM network to another or second LAN switch to a second LAN;wherein the LAN emulation means further comprises LAN emulation control hardware for presetting LAN switch controls in advance of the frame transmission for controlling the ATM network to function like a LAN when transporting frames from LANs to ATM or ATM to LANs;wherein the LAN emulation means further comprises a LAN emulation header means for identifying frames having information for presetting the LAN emulation control hardware;

~~The LAN emulation system of claim 29~~ wherein the LAN emulation control hardware further comprises a plurality of registers for storing LAN emulation headers, wherein each register contains a unique LAN emulation header data pattern.

31. (Original) The LAN emulation system of claim 30 wherein the plurality of registers specify the set of LAN emulation headers that contain information for presetting the LAN emulation control hardware.

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32. (Currently Amended) The LAN emulation system for claim 30 wherein the LAN emulation means further comprises a LAN emulation control sorting means for checking each LAN emulation header arriving from the ATM network to determine ~~if~~ if the LAN emulation header matches any of the prestored plurality of LAN emulation headers in the registers and contains information for presenting the LAN emulation control hardware.

33. (Original) The LAN emulation system of claim 32 wherein the LAN emulation means further comprises a forwarding means, wherein frames arriving from the ATM network containing information for presetting the LAN emulation control hardware are sent to the controlling processor to be processed.